REMARKS

Claims 1-9 and 19-24 are pending in the present application. Claims 1, 19 and 23 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Applicant notes that the drawings filed with the application papers have not been acknowledged in the Office Action. Acknowledgment of the drawings is respectfully requested.

Applicant notes with appreciation that the Office Action indicates at page 12 that claims 3-5, 7, 21-22 and 24 would be allowable if rewritten in independent form. Applicant wishes to defer submission of these claims, pending consideration of the present Amendment.

Claims 1, 6, 9, 19-20 and 23 stand rejected under 35 U.S.C. 102(e) as being anticipated by Suemura *et al.* (U.S. Patent No. 5,887,039 - hereinafter "Suemura"). Claim 8 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Suemura. Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Suemura in view of Sakamoto, *et al.* (U.S. Patent No. 6,557,110 - hereinafter "Sakamoto"). Reconsideration and removal of the rejections, and allowance of the claims, are respectfully requested.

The present invention of amended independent claim 1 is directed to an optical transfer system for converting an externally-applied video signal into an optical signal and for restoring the optical signal to the original video signal. A video controller separates color signals and a horizontal/vertical synchronous signal from an original video signal and transmits the color signals and the horizontal/vertical synchronous signal in response to an externally-applied predetermined data enable signal and clock signal. A transmitter includes a transmitter phase locked loop that, in response to a clock signal, generates a first plurality of non-overlapping clock signals of different respective phases. The transmitter skew-compensates signals received from the video controller, compresses the skew-compensated signals in response to the first plurality of non-overlapping clock signals, and converts the compressed signals to a driving current. A

transmission photo diode converts the driving current to an optical signal and outputs the optical signal. An optical transmission line comprised of a predetermined number of channels transmits the optical signal. A reception photo diode converts the optical signal received from the optical transmission line into a current signal and outputs the current signal. A receiver that includes a receiver phase locked loop that generates a second plurality of non-overlapping clock signals of different respective phases in response to a received clock included in the received optical signal converts the current signal into a voltage signal, decompresses the voltage signal in response to the second plurality of non-overlapping clock signals of different respective phases, compensates for the skew of the voltage signal, and restores the original signal.

The present invention of amended independent claim 19 is directed to a data restoration and skew compensation unit in a receiver having a phase locked loop for generating first through n-th non-overlapped clock signals, each having a predetermined offset and a different respective phase to prevent mutual overlapping. The receiver restores data in which n-bit synchronous signals (where n is a positive integer greater than or equal to 1) and n-bit information data are multiplexed and transmitted in series via a transmission channel, in response to the first through n-th non-overlapped clock signals. A first latch unit latches received serial data in units of n+N−1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to the first through n-th non-overlapped clock signals of different respective phases, and outputs N n-bit latched state data having the time difference of a predetermined offset there between. A second latch unit latches in parallel the N state data in response to an X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals. A synchronizer outputs state data from which the synchronous signal is detected, among data latched by the second latch unit, as restored information data, in response to a predetermined synchronous existence signal and the X-th non-overlapped clock signal.

The present invention of amended independent claim 23 is directed to a method of restoring information data from data in which n-bit synchronous signals (where n is a positive integer greater than or equal to 1) and the n-bit information data are multiplexed and transmitted

together with a clock signal in series via a transmission channel. First through n-th non-overlapped clock signals are generated, each having a predetermined offset and a different respective phase to prevent mutual overlapping, on the basis of the clock signal. Received serial data in units of n+N−1 (where N is a positive integer greater than or equal to 3) bits in parallel are latched in response to the first through n-th non-overlapped clock signals of different respective phases. N n-bit latched state data are generated having the time difference of a predetermined offset there between. The N state data are latched in parallel in synchronization with a X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals. State data is determined from which the synchronous signal is detected, among the latched state data, to be the restored information data, when the serial data is the synchronous signal.

In the present invention as claimed in amended independent claim 1, a "transmitter phase locked loop" generates a "first plurality of non-overlapping clock signals of different respective phases" and a "receiver phase locked loop" generates a "second plurality of non-overlapping clock signals of different respective phases." This feature is illustrated at least, for example, in FIGs. 2, 8, 15 and 17 of the present specification. In this example, a transmitter phase locked loop (PLL) 270, receives a clock signal CLK, generates a first plurality of non-overlapping clock signals CKP for data compression, and applies the non-overlapping clock signals CKP to the data serialization unit 240 (see FIG. 2 and page 8, lines 19-23 of the present specification). A receiver phase locked loop 88 receives a clock signal CLK from the optical receiver 80 and produces a second plurality of non-overlapping clock signals CKP for data decompression that is performed by the data restoration and skew compensation unit 82 (see FIG. 8 and page 20, lines 19-23 of the present specification). Each non-overlapping clock signal in the plurality of non-overlapping clock signals CKP is a signal whose phase has been shifted by the width P18 (see FIGs.15 and 17 and page 35, lines 18-19 of the present specification). Thus, the transmitter and receiver phase locked loop units 270, 88 each generate a set of "non-overlapped clock signals of different respective phases", the phases of which are offset by shifting the phase of the non-overlapped clock signals at intervals of the predetermined offset P18 (see FIGs. 15 and 17 and page 35, lines

20-22 of the present specification). The resulting non-overlapping clock signals are of substantially the same frequency, but of respectively different phases.

In addition, the "transmitter" compresses the "skew-compensated signals in response to the first plurality of non-overlapping clock signals", and the "receiver" decompresses the "voltage signal in response to the second plurality of non-overlapping clock signals." This feature is illustrated at least, for example, at FIGs. 2 and 8 of the present specification. In this example, the transmitter phase locked loop (PLL) 270 generates non-overlapping clock signals CKP that are used for data compression performed in the data serialization unit 240 (see FIG. 2 and page 8, lines 9-13 of the present specification). Also, the receiver PLL 88 provides non-overlapping clock signals CKP that are applied to the data restoration and skew compensation unit 82 for restoring the compressed data in response to the non-overlapping clock signals CKP (see FIG. 8 and page 20, line 21 to page 21, line 2 of the present specification).

In the present invention as claimed in amended independent claim 19, a "data restoration and skew compensation unit in a receiver having a phase locked loop" generates "first through n-th non-overlapped clock signals, each having a predetermined offset and a different respective phase to prevent mutual overlapping." In addition, a "first latch unit" latches "received serial data" in response to the "first through n-th non-overlapped clock signals of different respective phases." This feature is illustrated, at least at FIGs. 14-15 and 17 of the present specification, which include a "data restoration and skew compensation unit" 82 having a phase locked loop (PLL) 88, and generating "first through n-th non-overlapped clock signals each having a predetermined offset to prevent overlapping between them" (see FIGs. 14-15 and 17 and page 34, lines 1-3). The first latch unit 400 latches the data DATAIN in response to the "first through n-th non-overlapped clock signals of different respective phases" (see output "n" of PLL 88).

In the present invention as claimed in amended independent claim 23, "first through n-th non-overlapped clock signals" are generated, "each having a predetermined offset and a different respective phase to prevent mutual overlapping, on the basis of the clock signal." In addition, the

"received serial data" are latched "in response to the first through n-th non-overlapped clock signals of different respective phases." This feature, likewise, is illustrated, at least at FIGs. 14-15 and 17 of the present specification, as discussed above in conjunction with claim 19.

The Suemera reference is cited in the Office Action at page 6 as teaching a "...transmitter phase locked loop that, in response to a clock signal, generates a first plurality of non-overlapping clock signals...", and is further cited in the Office Action at page 7 as teaching "...a receiver that includes a receiver phase locked loop that generates a second plurality of non-overlapping clock signals... ." Suemera discloses a system and method for skew compensation that includes generating a transmission clock signal 36 at a transmitter by multiplying the frequency of an input clock signal 35 at a clock converter 42 (see Suemera, FIG. 5 and column 9, lines 35-37). Suemera includes synchronization pattern adders 11, into which data are written synchronously with the input clock signal 35, and out of which data are read synchronously with the transmission clock 36 (see Suemera FIG. 5 and column 9, lines 40-42). A second clock converter 44 at a receiver generates an output clock signal 37 by multiplying the frequency of the received and extracted transmission clock signal 36 (see Suemera, column 10, lines 45-49). The receiver further includes decoders 19, into which data are written synchronously with the transmission clock 36, and out of which data are output synchronously with the output clock signal 37. In addition, Suemera discloses a timing pulse generator 40 for generating a timing signal 30, which is input simultaneously to the four synchronization pattern adders (see Suemera, FIG. 5 and column 9, lines 47-49).

It is submitted that Suemera fails to teach or suggest the present invention as claimed in amended independent claim 1. In particular, Suemera fails to teach or suggest a "transmitter phase locked loop" that, in response to a clock signal, "generates a first plurality of non-overlapping clock signals of different respective phases." In Suemera, the input clock signal 35 is provided concurrently to multiple, parallel synchronization adders 11. The Office Action at page 3, lines 3-10 states that this is equivalent to providing "non-overlapping clock signals": "(parallel, which means non-overlapping clock signal)." However, while clock signals that are

distributed in parallel to multiple units technically do not "overlap" in the physical sense, they still do overlap in the electrical sense in that the signals themselves are of substantially equal phase. However, there is no discussion in Suemera that the parallel clock signals 35 provided to the multiple synchronization pattern adders are of "different respective phases", as claimed in claim 1 of the present invention. Therefore, it is submitted that this limitation is not met by Suemera. It is likewise submitted that the Suemera receiver does not include a "receiver phase locked loop" that generates "a second plurality of non-overlapping clock signals of different respective phases", for the reasons stated above. In addition, since the Suemera transmission clock signal 36 is a single signal that is generated by multiplying the frequency of an input clock signal, it follows that Suemera does not teach or suggest "a first plurality of non-overlapping clock signals" (emphasis added), as claimed in claim 1. Further, since Suemera generates a single output clock signal 37 by multiplying the frequency of the received transmission clock signal 36, it follows that Suemera does not teach or suggest "a second plurality of non-overlapping clock signals" (emphasis added), as claimed.

In addition, it is submitted that Suemera fails to teach or suggest a "transmitter..for compressing the skew-compensated signals in response to the first plurality of non-overlapping clock signals" (emphasis added) or a "receiver...for decompressing the voltage signal in response to the second plurality of non-overlapping clock signals" (emphasis added), as claimed in claim 1. Instead, in Suemera, each encoder 10 (believed to be asserted in the Office Action as providing a "compression" function) converts the 3-bit parallel data into 4-bit parallel data through 3B4B encoding (see Suemera, FIG. 8 and column 11, lines 12-14). The parallel data obtained through the encoding are then input to the synchronization pattern adders (see Suemera, column 11, lines 14-16). Since Suemera first encodes the 3-bit parallel data into 4-bit parallel data, then inputs the encoded data to the synchronization pattern adders, it follows that Suemera does not compress "the skew-compensated signals in response to the first plurality of non-overlapping clock signals" (emphasis added), and does not decompress "the voltage signal in response to the second plurality of non-overlapping clock signals" (emphasis added), as claimed.

In view of the above, it is respectfully submitted that Suemura fails to teach or suggest the invention as claimed in amended independent claim 1. Removal of the rejection and allowance of claim 1 are respectfully requested.

With regard to the rejection of independent claim 19, it is submitted that Suemura fails to teach or suggest a "data restoration and skew compensation unit in a receiver" that includes a "phase locked loop for generating first through n-th non-overlapped clock signals, each having a predetermined offset and a different respective phase to prevent mutual overlapping." As described above, Suemera does not teach or suggest generating "non-overlapped clock signals of different respective phases." Further, since Suemura fails to teach or suggest "first through n-th non-overlapped clock signals of different respective phases", it follows that Suemera fails to teach or suggest "latching in parallel the N state data in response to an X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals" (emphasis added), as claimed in amended independent claim 19. In view of the above, it is respectfully submitted that Suemura fails to anticipate amended independent claim 19. Removal of the rejection and allowance of claim 19 are respectfully requested.

With regard to the rejection of independent claim 23, it is submitted that Suemura fails to teach or suggest "generating first through n-th non-overlapped clock signals, each having a predetermined offset and a different respective phase to prevent mutual overlapping, on the basis of the clock signal"; or " latching in parallel the N state data in synchronization with a X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals" (emphasis added), for the reasons described above. In view of the above, it is respectfully submitted that Suemura fails to anticipate amended independent claim 23. Removal of the rejection and allowance of claim 23 are respectfully requested.

With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

Entry of the above amendments and allowance of all claims are respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

Date: August 26, 2004

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900, Ext. 4902
Facsimile: (617) 742-7774
J:\SAM\0143\082604 AAF\0143amendmentb.wpd

Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant